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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,909	03/24/2004	Sanjay Rekhi	10002.003310 (CD3016)	4004

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EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,909	REKHI ET AL.	
	Examiner	Art Unit	
	PHUC T. DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed June 17, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10,11,18 and 19* is/are rejected.

7)☒ Claim(s) *8-9 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's argument filed on June 17, 2005 with respect to claims 1-11 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1 and 18 are rejected under 35 U.S.C. 102 (b) as being anticipated by En (U.S. Patent No. 5,963,412).

Regarding claim 1, En discloses a method for providing a low voltage, high current plasma damage protection structure comprising:

coupling a first transistor (46, Fig. 3d) to a first metal wire on a first metal level (52, Fig. 3d) of a semiconductor device, the first transistor (46, Fig. 3d) being configured to protect a gate (42) of a second transistor (44, Fig. 3d) from charge buildup, a gate (G) of the first transistor (46, Figs. 3d) being left floating (col. 4, line 66)

forming a second metal wire (42, Fig. 3d) in the device; and

switching ON the first transistor (46, Fig. 3d) to discharge charges accumulated on the

first metal wire (52, Fig. 3d) during formation of the second metal wire (80, Fig. 3b) [col. 4, line 8-col. 5, line 56].

Regarding claim 18, En discloses a method for providing a low voltage, high current plasma damage protection structure, the method comprising:

switching ON a first transistor (46, Figs. 3d) to discharge charges accumulated on an interconnect line (52, Fig. 3d) during a metallization process to protect a gate (42) of a second transistor (44, Figs. 3d) coupled to the interconnect line (78), a gate (52) of the first transistor (46, Figs. 3d) being left floating during the metallization process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-5, 7,10and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over En in view of Eitan et al., hereinaher, "Eitan" (U.S. Publication No. U.S. 2001/0026970 A1).

Regarding claim 2, Eitan discloses a step of coupling the gate of the first transistor (52, Fig. 7) to ground (4 1, Fig. 7) on a topmost metal level of the device (Fig. 7).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

Regarding claim 3, Eitan discloses a second metal wire is on a second metal level of the

device, the second metal level being over the first metal level ((0057 page 4)).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

Regarding claim 4, Eitan discloses a step of coupling the first transistor to the first metal wire connecting a drain of the first transistor (52, Fig. 7) to the first metal wire (90, Fig. 7) connecting a source of the first transistor to ground (41, Fig. 7), and. connecting the gate of the first transistor (52, Fig. 7) to the metal wire (52, Fig. 7) by way of a coupling capacitor (120, Fig. 7).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

Regarding claim 5, Eitan discloses a value of the coupling capacitor is selected by design to switch ON the first transistor at a predetermined gate voltage ((0075) page 5).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

Regarding claim 7, Eitan discloses the second transistor comprises an MOS transistor ((0041) page 3).

It would have been obvious to one having ordinary skilled in the art at the time the

invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

Regarding claim 10, Eitan discloses the topmost metal level is a second metal level over the first metal level ((0057) page 4).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

Regarding claim 19, Eitan discloses a step of coupling the gate of the first transistor (52, Figs. 4a and 7) to ground (41, Figs. 4A and 7) after the metallization process.

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above teaching of Eitan to En discussed above for a purpose of preventing charge buildup in the process.

4. Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over En and Eitan in view of Ning (U.S. Patent No. 6,611,453).

En and Eitan discloses all the features of the claimed invention as discussed above, but does not disclose the second metal wire is formed in the metallization process comprises physical vapodeposition.

Ning, however, discloses the second metal wire is formed in the metallization process comprises physical vapor deposition (col. 5, lines 17-202.

It would have been obvious to one having ordinary skilled in the art at the time the

invention was made to modify the teaching of Ning to En and Eitan discussed above such that the second metal wire is formed in the metallization process comprises physical vapor deposition for a purpose of preventing charge buildup in the process.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over En and Eitan in view of Kuang et al., hereinafter, "Kuang" (U.S. Patent No. 6,281,737 B 1).

En and Eitan discloses all the features of the claimed invention as discussed above, but does not disclose the first transistor comprises an nfet.

Kuang, however, discloses the first transistor comprises an nfet (Abstract).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Kuang to En and Eitan discussed above such that the first transistor comprises nfet for a purpose of preventing parasitic current can occur.

Allowable Subject Matter

6. The following is a statement of reason for the indication of allowable subject matter:

Claims 8-9, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the Prior Art made of record discloses a step of forming a second metal level over the first metal level; forming a third metal level over the second metal level; and coupling the gate of the first transistor to a third metal wire on the third metal level by way of a plurality of vertically stacked vias as cited in claim 8 and the metallization process comprises physical vapor deposition as cited in claim 20.

Claim 9 is depend on claim 8, then, it also would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:O0 pm.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300 for regular communications and after Final communications.

9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PP

Primary Examiner

Art Unit 28 18